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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RIAD, AMINE	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,792	LAI ET AL.	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 15-20* is/are rejected.

7)☒ Claim(s) *7-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claims 1-20 have been submitted for examination.

Claims 1-6,15-20 have been rejected.

Claims 7-14 have been objected to.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Olarig U.S Patent 6,038,680.

In regard to claim 1,

Oralig discloses a computer system, unaffected by memory module instability, comprising:

- Memory mirror unit controlling (Figure 1;Item 29) a plurality of memory modules (Figure 1; items 55a and 55b) and receiving an error control signal (Figure 1; item 27a), wherein each of the memory mirror units writes data to the corresponding memory modules during a write cycle (Column 7; lines 10-12)

- Activates a first memory module among the memory modules, reading data during a read cycle; (Column 6; lines 30-32)[Olarig discloses that the module is deactivated. [Examiner points out that in order for a memory module to be deactivated it has to be activated first during a read cycle]

- Memory controller enabling the error control signal upon detection of a read error in the first memory module (Column 7; lines 6-7), wherein the memory mirror unit

disables the first memory module and activates a second memory module among the memory modules when the read error occurs in the first memory module.(Column 7; lines 8-13)

In regard to claim 2

Olarig discloses the computer system as claimed in claim 1, further comprising:

- A central processing unit (CPU); (Figure 2; item 10)
- A system interruption device providing an interruption signal to the CPU to interrupt system operations and then activate the corresponding error control signal when the memory controller detects the read error. (Figure 1; item 19 NMI non maskable interrupt)

In regard to claim 3,

Oralig discloses the computer system as claimed in claim 2, wherein each memory mirror unit receives a corresponding error control signal for control of corresponding memory modules.(Column 6; lines 33-35) ["By rerouting signals from the controller to the auxiliary connector a problem can be eliminated" this means that an error signal was initially routed from the auxiliary module to the control unit for error declaration]

In regard to claims 4, 16, and 19

Oralig discloses the computer system as claimed in claim 3, wherein the memory controller determines that the read error has occurred when the memory controller

detects an irreparable error in the first memory module of corresponding memory modules during the read cycle. (Column 4; lines 38-47) [Item 27a where the ECC takes place is connected with item 29 through line 33, and that shows the how the controller is connected to the corresponding memory module]

In regard to claims 5, 17, and 20

Oralig discloses the computer system as claimed in claim 3, wherein the memory controller determines that the read error has occurred when the memory controller detects that the number of errors in the first memory module reaches a predetermined value. (Column 6; lines 64-67) & (Column 7; lines 1-3)

In regard to claims 15, and 18

Oralig discloses a method for controlling memory of a computer system, the method comprising the steps of:

- Providing at least one memory mirror unit,(Figure 1; item 29) each controlling a memory module group having a plurality of memory modules; (Figure 1; items 55b and 55a)
- Equalizing addresses of the memory modules inside each memory module group; (Column 2; lines 48-55)
- Writing data to the corresponding memory modules according to a write address during a write cycle; Reading a first memory module according to a read address during a read cycle; (Column 7; lines 10-13)

- The computer system activates an error control signal (Column 7; lines 6) received by the corresponding memory mirror unit to select a second memory module from corresponding memory modules when a read error occurs in the first memory module. (Column 7; line 8 [hot swap is considered the switch to the mirrored memory module])

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable in view of Oralig U.S Patent 6,038,680 over Ohran Patent Application Publication 2002/0099916.

Oralig discloses the computer system of parent claims 3 and 1 where the controller activates the error control signal and the memory mirror unit only activates the second memory module upon detection of the read error in the first memory module during the read cycle. (Column 7; 6-12)

Oralig does not disclose that the memory mirror unit activates the first and second memory module during the write cycle, and only activates the first memory module during the read cycle.

Ohran teaches that:

- The memory mirror unit activates the first and second memory module during the write cycle ,(Page 1; Paragraph 13;"for each write request, a copy of the request is written into the backup system") [Requests here are equivalent to activating]
- Only activates the first memory module during the read cycle. (Page 3; Paragraph 31; "A read operation is performed by the primary computer") [Requests here are equivalent to activating]

It would have been obvious to one of ordinary skill in the art at the time the invention to implement the activation of the first and second memory module during a write cycle, and activating the first memory module during the read cycle of Ohara into the computer system of Oralig.

One of ordinary skill in the art would have been motivated to make this modification because mirroring allows recovery from failures as disclosed by Ohara (Page 1; Paragraph 7)

Allowable Subject Matter

Claims 7-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant s invention. Patent Application Publication 2003/0090941 covers mirroring data within

memory, but lacks hardware components essential to the Application.

See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR
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Patent Examiner
7/12/2006

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